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|-----------------------------------|---------------------------------------|--|-------------|
| Notice of References Cited | Application/Control No. 09/695,756 | Applicant(s)/Patent Under Reexamination VOSHEL | |
| | Examiner Guy J. Lamarre, P.E. | Art Unit 2133 | Page 1 of 1 |

U.S. PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|--|-----------------|-------------------|----------------|
| * | A | US-4,642,793 | 02-1987 | Meaden, Dan F. | 711/216 |
| * | B | US-5,659,737 | 08-1997 | Matsuda, Yasuhiro | 341/90 |
| * | C | US-6,374,250 | 04-2002 | Ajtai et al. | 341/50 |
| * | D | US-5,881,221 | 03-1999 | Hoang et al. | 714/38 |
| * | E | US-5,363,382 | 11-1994 | Tsukakoshi, Hisao | 714/711 |
| * | F | US-4,558,302 | 12-1985 | Welch, Terry A. | 341/51 |
| * | G | US-4,979,039 | 12-1990 | Kisor et al. | 341/106 |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

FOREIGN PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|--|-----------------|---------|------|----------------|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) | | | |
|---|---|---|--|--|--|
| * | U | NN8806199(Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory; IBM Technical Disclosure Bulletin, June 1988, US; VOLUME NUMBER: 31, PAGE NUMBER: 199 - 202) | | | |
| | V | Hancu et al. "A concurrent test architecture for massively parallel computers and its error detection capability; IEEE Transactions on Parallel and Distributed Systems, Page(s): 1169 –1184, Vol. 5, Issue: 11; Nov, 1994" | | | |
| | W | Sakai et al. 'A wafer scale fail bit analysis system for VLSI memory yield Improvement; Proceedings of the 1990 International Conference on Microelectronic Test Structures, ICMTS 1990; Page(s): 175 –178, 7 Mar 1990" | | | |
| | X | | | | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.